WHAT IS CLAIMED IS:

1. An integrated circuit comprising a plurality of dynamically adjustable impedance termination circuits that are coupled together in parallel to a first pin, each of the impedance termination circuits comprising:

first resistors coupled in parallel;

a second resistor coupled in series with the first resistors;

first pass gates each coupled in series with one of the first resistors and each coupled to a first control signal; and

a second pass gate coupled to the first pass gates and coupled to receive a second control signal.

2. The integrated circuit according to claim 1 wherein the first resistors comprise three resistors coupled in parallel.

3. The integrated circuit according to claim 1 wherein the integrated circuit comprises three of the impedance termination circuits coupled together in parallel to the first pin.

4. The integrated circuit according to claim 1 wherein each of the first pass gates and the second pass gates comprise a p-channel transistor and an n-channel transistor coupled together in parallel.

5. The integrated circuit according to claim 1 wherein the integrated circuit includes a second set of impedance termination circuits that are coupled together in parallel to a second pin, the first and the second pin being differential input/output pins.

6. A method for providing dynamically adjustable on-chip termination impedance to a first input/output pin on an integrated circuit, the method comprising:

controlling first current paths through first on-chip resistors that coupled together in parallel using first pass gates, each first pass gate being coupled in series with one of the first on-chip resistors;

providing a second current path through the first on-chip resistors and a second on-chip resistor that is coupled in series with the first on-chip resistors by turning ON a second pass gate;

providing a third current path through a third on-chip resistor that is coupled in parallel with the first and the second on-chip resistors by turning ON a third pass gate, wherein the second and the third resistors are coupled to the first pin;

sensing the on-chip termination impedance; and

dynamically adjusting the on-chip termination impedance by changing states of the first pass gates.

7. The method of claim 6 further comprising:

coupling fourth on-chip resistors together in parallel by turning ON fourth pass gates, each fourth pass gate being coupled in series with one of the fourth resistors,

wherein the fourth on-chip resistors are coupled in series with the third resistor and the second current path flows through the fourth resistors.

8. The method of claim 7 further comprising:

blocking current through a fifth resistor coupled in parallel with the first and the second on-chip resistors by turn OFF a fifth pass gate.

9. The method of claim 7 further comprising:

blocking current through a selected one of the fourth resistors by turning OFF one of the fourth pass gates that is coupled to the selected fourth resistor.

10. The method of claim 6 further comprising:

blocking current through a selected one of the first resistors by turning OFF one of the first pass gates that is coupled the selected first resistor.

11. The method of claim 6 further comprising:

decoupling a third on-chip resistor from the first on-chip resistors by turning OFF a third pass gate; and

blocking a fourth current path through a fourth on-chip resistor that is coupled in parallel with the first and the second on-chip resistors by turning OFF a fourth pass gate.

12. The method of claim 6 wherein the integrated circuit is a field programmable gate array.

13. The method of claim 6 further comprising providing on-chip termination impedance to a second input/output pin on the integrated circuit by:

coupling fourth on-chip resistors together in parallel by turning ON fourth pass gates, each fourth pass gate being coupled in series with one of the fourth on-chip resistors;

providing a fourth current path through the fourth on-chip resistors and a fifth on-chip resistor coupled in series with the fourth on-chip resistors by turning ON a fifth pass gate,

wherein the first and the second pins are differential pins.

14. An integrated circuit comprising a first dynamically adjustable on-chip impedance termination circuit, wherein the first impedance termination circuit comprises:

means for coupling together first resistors in parallel in response to first control signals;

means for providing a first current path through a second resistor coupled in series with the first resistors in response to a second control signal; and

means for providing a second current path through a third resistor coupled in parallel with the first resistors and the second resistor in response to a third control signal, wherein the first, second, and third resistors provide termination impedance at a pin.

15. The integrated circuit as defined in claim 14 further comprising:

means for blocking current through a fourth on-chip resistor that is coupled to the second and the third on-chip resistors in response to a fourth control signal.

16. The integrated circuit as defined in claim 14 further comprising:

means for blocking current flow through one of the first resistors in response to a changed value of a corresponding one of the first control signals.

17. The integrated circuit as defined in claim 14 wherein the integrated circuit further comprises a second on-chip impedance termination circuit coupled to the first on-chip impedance termination circuit, wherein the second impedance termination circuit comprises:

means for coupling together fourth resistors in parallel in response to fourth control signals;

means for providing a third current path through a fifth resistor coupled in series with the fourth resistors in response to a fifth control signal; and

means for providing a fourth current path through a sixth resistor coupled parallel with the fourth resistors and the fifth resistor in response to a sixth control signal, wherein the fourth, fifth, and sixth resistors provide termination impedance at a second pin.

18. The integrated circuit as defined in claim 14 wherein the integrated circuit is a programmable logic device.

19. The integrated circuit as defined in claim 14 further comprising:

means for coupling together fourth resistors in parallel in response to fourth control signals, wherein the second current path flows through the third and the fourth resistors.

20. The integrated circuit as defined in claim 19 further comprising:

means for providing a third current path through a fifth resistor coupled parallel with the fourth and the third resistors in response to a fifth control signal.